World Scientific Research Journal (WSRJ) ISSN: 2472-3703
www.wsr-j.org

Design of Power Amplifier based on DMR Transmitter Applications

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Abstract: In this paper, a cascade power amplifier used in the radio frequency front-end of DMR transmitter is designed. The integrated power amplifier chip of Agilent Company is adopted in this design, and its peripheral circuit is designed to achieve the characteristics of miniaturization. The cascade power amplifier is simulated by Advanced Design System. The circuit chooses FR4 as a dielectric substrate. The test results show that S21 is more than 15dB in 430mHz-460mHz.

Keywords: cascade power amplifier, power amplifier chip, miniaturization.

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1. INTRODUCTION

Compared with other standard of trunking communication, DMR (Digital Mobile Radio) digital trunking communication system has the advantages of low cost, higher openness and high spectral efficiency. It has been widely recognized by the global communications industry today [1]. The radio frequency (RF) electronic technology is the basis of contemporary mobile communications, in order to achieve effective wireless transmission and the small size of mobile terminals. The modern mobile communications inevitably place higher demands on radio frequency technologies. Therefore, the research on RF technology is not only the key point but also the difficult point in modern mobile communication. Its research has broad prospects. Among them, the power amplifier is an important part of the DMR transmitter RF front-end. So it is important to design a miniaturized, gain-stable power amplifier.

In the RF transmitter, the power of the modulated signal is very small, about 0dBm. In order to radiate the modulated signal through the antenna, it is necessary for the power amplifier to amplify the signal to the specified power in order to meet the needs of wireless communication. Because in the RF transmitter amplifier circuit, it is difficult to amplify the signal with a zoom to the specified power, the general need to use two amplifications, or even three amplification circuit to amplify the signal, so that the match between the class is particularly important. At the same time, the system structure should be simplified as much as possible and the volume of transmitter system should be reduced.

In order to meet the RF transmit power and small size of the system requirements, the design uses integrated power amplifier chip to meet the gain, linearity and miniaturization requirements. Considering its gain, linearity and input power, the power amplifier selects two integrated chips with excellent gain and stable output power with temperature variation, namely HMC480ST89 and HMC453ST89 respectively. Using Advanced Design System (ADS) software to simulate each power amplifier chip separately, after the working frequency, gain and linearity meet the requirements [2]. Then two power amplifier chip cascaded simulation, and optimize it to meet the target requirements, and the design of printed circuit boards. The test results show that S21 is more than 15dB in 430mHz-460mHz.

2. DRIVER STAGE POWER AMPLIFIER CIRCUIT DESIGN

The driver stage RF amplifier circuit is mainly used to amplify the RF signal output from the voltage-controlled oscillator of the RF front end of the transmitter. For the transmission path, it is to provide a certain intensity of excitation signal for the rear stage amplifier. The driving stage amplifier chooses the HMC480ST89 DC-5GHz InGap HBT gain block MMIC amplifier of Hittite company. The typical gain of HMC480ST89 in DC-5GHz band is 19dB, the static working current is 82mA and the output 1dB compression point is 22dBm [3]. The circuit chooses FR4 as a dielectric substrate, dielectric constant 4.2, medium thickness 1.58mm, and characteristic impedance is 50Ω. The internal input and output impedance of HMC480ST89 has been matched to 50 Ω, so no additional impedance matching network is required. The circuit design is shown in figure 1.

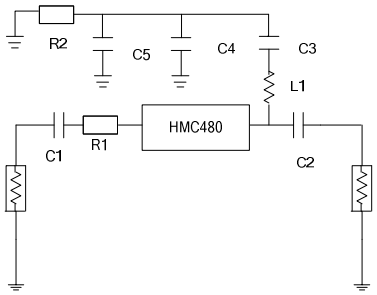


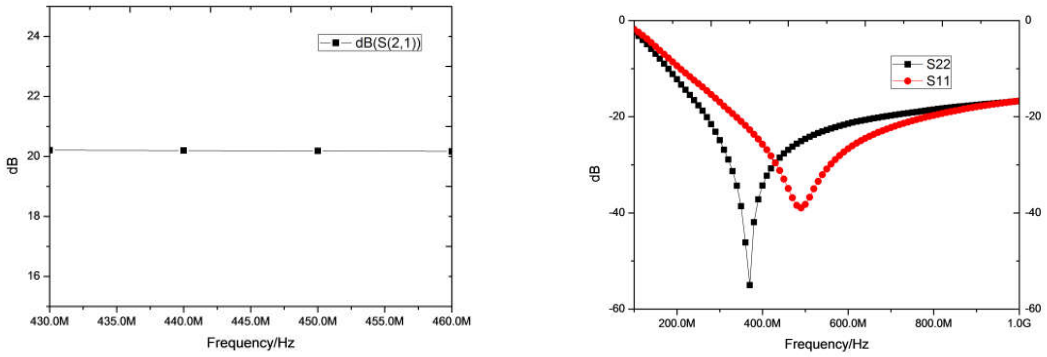
Fig. 1 Circuit schematic of driver stage power amplifier.

C3, C4, C5, L1 constitute a bias network. The bias network realizes the DC feed of the circuit, and at the same time, it is necessary to prevent the RF signal from entering the DC power supply. L1 is the choke inductance, it allows DC signal to pass, but Prevent the AC signal from passing. R2 is the bias resistance and R resistance selection meets the formula 1.

$$R2 = (V_s - V_{cc}) / I_{cc} \tag{1}$$

Where Vs = 8V, Vcc = 5V, Icc = 82mA, then can be calculated R2 = 39Ω.

C1 and C2 are coupling capacitors, which block current and coupling AC signals. In 430mHz-460mHz, the capacitance of the coupling capacitance should not be too small, and the capacity of the coupling capacitor is 100pF. Another important parameter of power amplifier is stability. In the simulation, the stability is less than 1, that is, the power transistor is unstable in the whole band. At this point, a small resistor R1 is attached behind the input capacitor. The S parameters of the driver stage power amplifier are simulated, and S21 and S11, S22 are obtained as shown in the figure 2 (a), (b) respectively. The simulation results show that S21 is more than 20.5dB, S11, S22 are lower than -20dB in 430mHz-460mHz.



(a) (b)

Fig. 2 The S parameters simulation of the drive stage power amplifier.

3. FINAL STAGE POWER AMPLIFIER CIRCUIT DESIGN

The final RF Power Amplifier is the most important and key stage of the transmitter. The output power, efficiency and stability of the last stage amplifier are basically equal to the output power and efficiency of the transmitter. HMC453ST89 is used in the final stage power amplifier. It is high dynamic range GaAs InGaP HBT 1.6Watt MMIC power amplifiers operating from 0.4 to 2.2GHz. The output 1dB compression point is 32 dBm, the power gain is 19 dB in the 450 MHz – 496 MHz [4]. By adjusting the size of matching network capacitors, the circuit work in 430 MHz -460 MHz. The circuit chooses FR4 as a dielectric substrate, dielectric constant 4.2, medium thickness 1.58mm, and characteristic impedance is 50Ω. The circuit design is shown in figure. 3

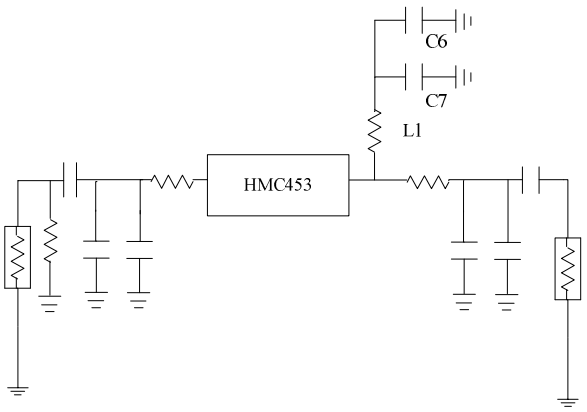
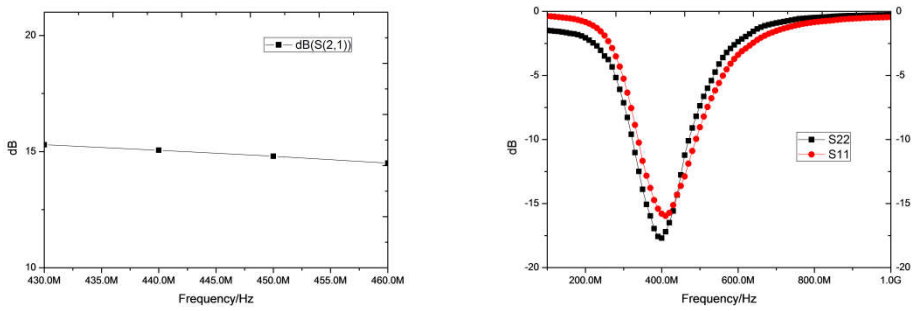


Fig. 3 Circuit schematic of final stage power amplifier.

C6, C7, L1constitute a bias network. The function of bypass capacitor C6, C7 is to suppress the high-frequency harmonics of DC power supply at different frequencies. L1 is the choke inductance, it allows DC signal to pass, but Prevent the AC signal from passing. The S parameters of the final power amplifier are simulated, and S21 and S11, S22 are obtained as shown in the figure 4 (a), (b) respectively. The simulation results show that S21 is more than 15dB, S11, S22 are lower than -15dB in 430mHz-460mHz.



(a) (b)

Fig. 4 The S parameters simulation of the final stage power amplifier.

4. CASCADE POWER AMPLIFIER CIRCUIT SIMULATION AND ANALYSIS

Two-stage power amplifier cascade directly through the 50Ω microstrip line, by adjusting the parameters of the matching network, the cascaded amplifier circuit to meet the requirements. The cascade power amplifier Photograph is shown in figure 5. The cascade circuit is tested by Agilent's vector network analyzer. The simulated and measured S21 of the cascaded power amplifier is shown in Figure. 6

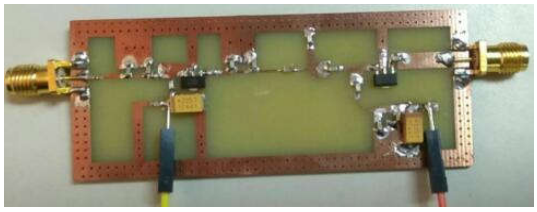


Fig. 5 Photograph of cascaded power amplifier

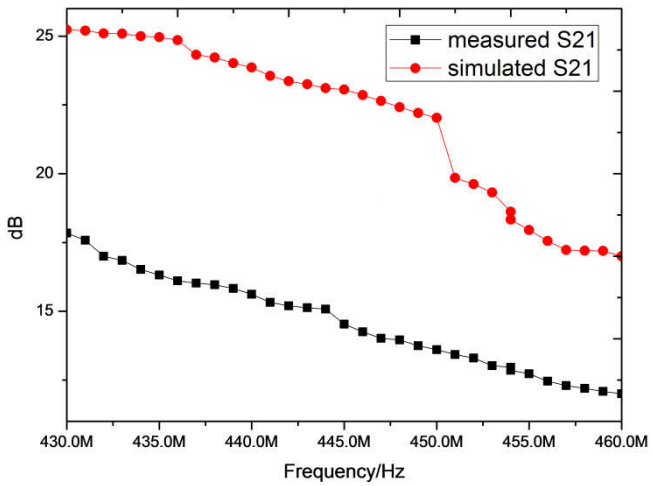


Fig. 6 Simulated and Measured S21 of the cascaded power amplifier

It can be seen that there is a certain deviation between the test results and the simulation results, which may have a certain effect on the circuit welding and test environment.

5. CONCLUSION

In this paper, a cascade power amplifier used in the RF front-end of DMR transmitter is designed. The use of integrated amplifier chip to achieve the characteristics of miniaturization. The test results show that S21 is more than 15dB in 430mHz-460mHz. The cascade power amplifier circuit can be used in RF front-end circuit of DMR transmitter.

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